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| EXAMINER |
|---|
| LOKE, STEVEN HO YIN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/061,475 | KRUTSICK, THOMAS J. | |
| | Examiner | Art Unit | |
| | Steven Loke | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *14 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 9-13* is/are rejected.

7)☒ Claim(s) *5,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Claims 14-15 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

2. Applicant's election without traverse of claims 1-13 in Paper No. 7 is acknowledged.

3. The abstract is objected to because of the following informalities: line 5, the phrase "...the first transistor if formed..." is unclear whether it is being referred to "...the first transistor is formed...".

Appropriate correction is required.

4. The disclosure is objected to because of the following informalities: There is no dielectric layer [1302] (page 15, line 20) in fig. 13 and an upper surface [1300] (page 15, line 21) in fig. 13. There is no upper surface [1400] (page 17, line 7) in fig. 14.

Appropriate correction is required.

5. Claims 2, 3, 7 and 8 are objected to because of the following informalities: Claim 2, line 4, claim 3, line 4, claim 7, lines 3-4, claim 8, lines 13-14, the phrase "an upper surface of the semiconductor wafer" is unclear whether it is being referred to the upper surface of the semiconductor wafer of claim 1. Claim 3, line 1, the phrase "the at least one dielectric spacer" has no antecedent basis; lines 3-4, the phrase "the upper surface of the substrate" has no antecedent basis. Appropriate correction is required.

6. Claims 3, 11 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3, lines 5-6, the phrase "etching the semiconductor wafer until the oxide layer on a horizontal portion of the semiconductor wafer is substantially removed" is unclear. The specification discloses after anisotropic etching has been completed, the silicon dioxide layer on the horizontal portions of the wafer will be removed and the silicon dioxide layer on the sidewalls of the corresponding electrodes 500, 502, 504 will remain (page 11, lines 4). It is believed that the oxide layer is being etched until the oxide layer on a horizontal portion of the semiconductor wafer is substantially removed in claim 3.

OK

Claim 11, lines 2-3, the phrase "forming a dielectric layer on the semiconductor wafer such that an upper surface of the semiconductor wafer is substantially planar" is unclear. Fig. 13 shows the dielectric layer [302] having a planar upper surface [300]. It is believed that a dielectric layer is being formed on the semiconductor wafer such that an upper surface of the dielectric layer is substantially planar.

Claim 13, line 3, the phrase "predetermined characteristics of the complementary bipolar transistors are set to a desired value" is unclear as to what characteristics of the complementary bipolar transistors are set to a desired value.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4, 9, 12 and 13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Miwa.

In regards to claim 1, Miwa shows all the elements of the claimed invention in figs. 1A-1I. It discloses a method of fabricating complementary bipolar transistors [NPN1, PNP2] on a semiconductor wafer [11, 14], the method comprising the steps of: forming a first electrode [20N] corresponding to a first transistor [NPN1], and a second electrode [20P] corresponding to a second transistor [PNP2] which is complementary to the first transistor, the first and second electrodes being formed on an upper surface of the semiconductor wafer; selectively introducing a first impurity into the first and second electrodes (col. 4, lines 10-24); forming a third electrode [24N] corresponding to the first transistor [NPN1], the third electrode being self-aligned with and electrically isolated from the first electrode [20N] (col. 5, lines 25-30), and forming a fourth electrode [24P] corresponding to the second transistor [PNP2], the fourth electrode being self-aligned with and electrically isolated from the second electrode [20P] (col. 5, lines 25-30); selectively introducing a second impurity into the third and fourth electrodes (col. 4, lines 49-60); forming a first active region [25] of the first transistor [NPN1] and a first active region [26] of the second transistor [PNP2], whereby at least a portion of the first impurity associated with the first and second electrodes [20N, 20P] diffuses into the first active regions of the first and second transistors (col. 4, lines 61-67); and forming a second active region [27] of the first transistor [NPN1] and a second active region [28] of the second transistor [PNP2], whereby at least a portion of the second impurity associated with the third and fourth electrodes [24N, 24P] diffuses into the second active regions of the first and second transistors (col. 4, line 61 to col. 5, line 4).

In regards to claim 2, Miwa further discloses the step of forming a dielectric spacer [23N, 23P] on a vertical sidewall portion of each of at least the first and second electrodes [20N, 20P], the dielectric spacers electrically isolating at least the first and second electrodes from an adjacent structure formed on the upper surface of the semiconductor wafer (col. 4, lines 37-47).

In regards to claim 3, Miwa further discloses the step of forming the at least one dielectric spacer [23N, 23P] comprises the step of: depositing an oxide layer on the upper surface of the semiconductor wafer. It is inherent to include a step of etching the oxide layer until the oxide layer on a horizontal portion of the semiconductor wafer is substantially removed and the oxide layer substantially remains on the sidewall portions of at least the first and second electrodes because there is only one oxide layer depositing on the semiconductor substrate.

In regards to claim 4, Miwa (fig. 1D) further discloses the step of forming the first and second electrodes comprises the steps of: forming a first polysilicon layer [20] on the upper surface of the semiconductor wafer; forming an oxide insulating layer [21] on the first polysilicon layer; selectively patterning the oxide layer [21] to define predetermined areas of the first polysilicon layer to be etched; and etching away the predetermined areas of the first polysilicon layer (col. 4, lines 10-24). It is inherent that the oxide layer [21] is a hard mask because it is a well-known hard mask material.

In regards to claim 9, Miwa further discloses the step of selectively introducing the first impurity into the first and second electrodes comprising the first and second electrodes with a predetermined concentration of the first impurity (col. 4, lines 10-24).

In regards to claim 12, Miwa further discloses the step of selectively introducing the second impurity into the third and fourth electrodes comprising the third and fourth electrodes with a predetermined concentration of the second impurity (col. 4, lines 49-60).

In regards to claim 13, Miwa further discloses a step of: performing a controlled rapid thermal anneal on the semiconductor wafer (col. 4, line 61 to col. 5, line 4), whereby the resistances of the emitter and base regions of the complementary bipolar transistors [NPN1, PNP2] are set to a desired value.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miwa.

In regards to claim 6, Miwa shows forming a second polysilicon layer [24] on the upper surface of the semiconductor wafer. Miwa differs from the claimed invention by not showing forming a hard mask layer on the second polysilicon layer; selectively patterning the hard mask layer to define predetermined areas of the second polysilicon layer to be etched; and etching away the predetermined areas of the second polysilicon layer. It would have been obvious to form a hard mask layer on the second polysilicon layer; selectively patterning the hard mask layer to define predetermined areas of the second polysilicon layer to be etched; and etching away the predetermined areas of the second polysilicon layer because all etching process would require a patterned hard

mask layer to determine the desired portion(s) of the underlying layer that are going to be etched.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miwa in view of Gomi.

Miwa differs from the claimed invention by not showing the step of forming a silicide layer on an upper surface of at least one electrode associated with the complementary transistors, the silicide layer providing a substantially low ohmic connection with a corresponding electrode.

Gomi (col. 13, lines 26-40) discloses the step of forming a silicide layer (AlSi) [68En] on an upper surface of at least one electrode [63En] associated with the complementary transistors [V-NPNTr, V-PNPTr] in fig. 3M.

It is inherent that the silicide layer [68En] providing a substantially low ohmic connection with a corresponding electrode [63En] because AlSi has low electrical resistance.

Since both Miwa and Gomi teach complementary bipolar transistors with a polysilicon emitter electrode, it would have been obvious to have the silicide ohmic electrode of Gomi in Miwa because it provides connection between the polysilicon electrode and the external circuit.

12. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claim 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

14. Claims 7 and 8 would be allowable if rewritten to overcome the objections set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is the step of forming the first and second electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing residual oxide between the first polysilicon layer and the upper surface of the semiconductor wafer. The second major difference in the claims not found in the prior art of record is the step of performing a blanket etch-back of the semiconductor wafer until at least a portion of each of the dielectric spacers on the sidewalls of the first and second electrodes is detected at the upper surface of the semiconductor wafer. The third major difference in the claim not found in the prior art of record is the steps of forming a dielectric layer on the semiconductor wafer such that an upper surface of the dielectric layer is substantially planar; forming a plurality of contact windows at predetermined areas in the dielectric layer; depositing a conductive layer on the upper surface of the semiconductor wafer; and selectively patterning the conductive layer to form a plurality of contacts, the contacts being electrically connected to respective electrodes associated with the complementary bipolar transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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April 6, 2003

Steven Loke
Primary Examiner